WE CLAIM:

1. A signal strength indicator circuit, comprising:

a first amplifier stage for receiving a first input signal from a first mixer and a second input signal from a second mixer;

a second amplifier stage for receiving a first set of differential inputs from the first amplifier stage;

a third amplifier stage for receiving a second set of differential inputs from the second amplifier stage; and

an output port for emitting an output signal that is a rectified combination of the first input signal and the second input signal.

2. The circuit of claim 1, wherein the first amplifier stage is also for receiving a third signal from a DC offset cancellation loop.

3. The circuit of claim 1, wherein the second amplifier stage and the third amplifier stage each provide a substantially similar amount of amplification.

4. The circuit of claim 1, wherein the first amplifier stage provides a higher amount of amplification than each of the second amplifier stage and the third amplifier stage provide individually.

5. The circuit of claim 1, wherein the first amplifier stage provides a higher gain than either of the second amplifier stage and the third amplifier stage so as to compensate for receiving the first input signal and the second input signal individually, while the second amplifier stage and the third amplifier stage each receive signals that are combinations of the first input signal and the second input signal.

6. The circuit of claim 5, wherein the first amplifier stage provides a first gain that is at least 3dB higher than either a second gain from the second amplifier stage and a third gain from the third amplifier stage.

7. The circuit of claim 1, wherein the first amplifier stage, the second amplifier stage, and the third amplifier stage are each biased to draw a same amount of current and to operate at a same voltage level.

8. A method of processing signals input into a signal strength indicator circuit, the method comprising:

a first receiving step wherein a first input signal is received from a first mixer and a second input signal is received from a second mixer in a first amplifier;

a forwarding step wherein a first set of differential inputs are forwarded from the first amplifier to a second amplifier and wherein a second set of differential inputs are forwarded from the second amplifier to a third amplifier; and

an emitting step wherein an output signal that is a rectified combination of the first input signal and the second input signal is emitted from the circuit.

9. The method of claim 8, further comprising a second receiving step wherein a third signal is received in the first amplifier from a DC offset cancellation loop.

10. The method of claim 8, further comprising a first amplifying step wherein the second amplifier and the third amplifier amplify the first

set of differential inputs and the second set of differential inputs in substantially similar amounts.

11. The method of claim 10, further comprising a second amplifying step wherein the first amplifier amplifies a combination of the first input signal and the second input signal in a greater amount than the substantially similar amounts that the second amplifier and the second amplifier amplify the first and second sets of differential inputs.

12. The method of claim 8, further comprising the step of biasing the first amplifier, the second amplifier, and the third amplifier such that each draws a same amount of current and operates at a same voltage level.

13. The method of claim 8, wherein the emitting step comprises the rectified combination includes all information contained in the first input signal and the second input signal.

14. The method of claim 8, wherein the emitting step comprises sending the second input signal to a comparator and emitting an output indicator to cause gain switching in an amplifier.

15. A signal strength indicator circuit, comprising:

a first amplifying means for receiving a first input signal from a first mixer and a second input signal from a second mixer;

a second amplifying means for receiving a first set of differential inputs from the first amplifying means;

a third amplifying means for receiving a second set of differential inputs from the second amplifying means; and

an emitting means for emitting an output signal that is a rectified combination of the first input signal and the second input signal.

16. The circuit of claim 15, wherein the first amplifier stage is also configured to receive a third signal from a DC offset cancellation loop.

17. The circuit of claim 15 wherein the second amplifying means and the third amplifying means each provide a substantially similar amount of amplification.

18. The circuit of claim 15, wherein the first amplifying means provides a higher amount of amplification than each of the second amplifying means and the third amplifying means provide individually.

19. The circuit of claim 15, wherein the first amplifying means provides a higher gain than either of the second amplifying means and the third amplifying means so as to compensate for receiving the first input signal and the second input signal individually, while the second amplifying means and the third amplifying means each receive signals that are combinations of the first input signal and the second input signal.

20. The circuit of claim 19, wherein the first amplifying means provides a first gain that is at least 3dB higher than either a second gain from the second amplifying means and a third gain from the third amplifying means.

21. The circuit of claim 15, wherein the first amplifying means, the second amplifying means, and the third amplifying means are each biased to draw the same amount of current and the same voltage level.